

Appl. No. 09/722,664 Atty. Dkt.: 723-969 Amdt. dated March 2, 2004 REPLACEMENT SHEET MAR O 2 DOW 702 Pixel Engine 700 digital RGB Display 56 Texture Environment Unit 909 Display Controller/ Video Interface Graphics Memory Request Arbitration 131 3D graphics Pipeline TMEM 500 Texture Unit 164 154 <u> 205</u> Setup/ Rasterizer 400 Transform Unit 300 81 Cache/ Command Processor 200 134 Memory Interface/ Controller Processor Interface 150 Main Memory 112 External Storage ## E 2-Level gather Buffer Cache Write-Main Processor ₁



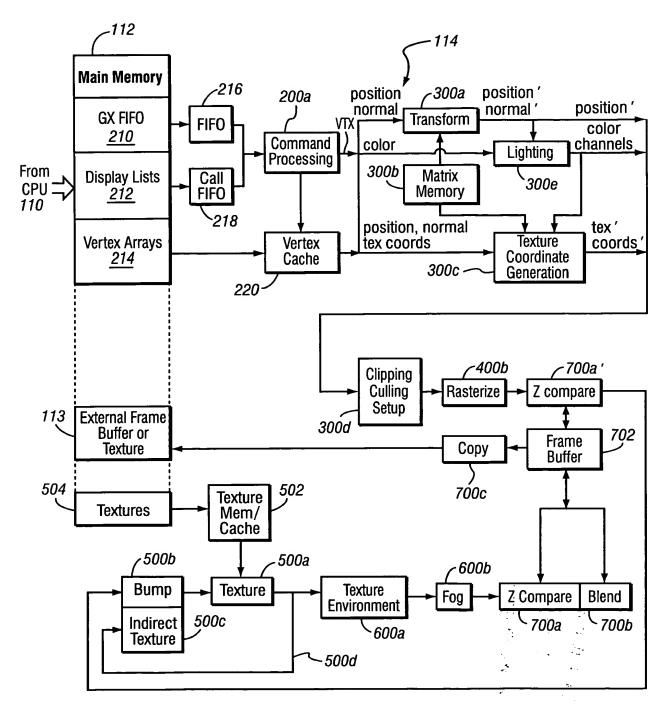


Fig. 5 EXAMPLE GRAPHICS PROCESSOR FLOW

Fig. 6 EXAMPLE INPUT/OUTPUT SUBSYSTEM 904 I/O Subsystem ,1000 SID 1[3:0] SID 0[3:0] Bus Serial To/From I/F I/F 52 SI PIINT **eDRAM** 132,142 -1100 902 **EXI** I/F EXI_PIINT EXI2DI EXI2CLK EXI2CSb EXI2INTb DICOVER
DIERRB
DIDI7:0]
DIDIR
DIHSTRBB
DIDSTRBB
DIBRK
DIRSTB 1200 **GFX GFX Regs** unit Disk To/From 180 I/F 106 DI PIINT AID0 ,1300 Audio To/From I/F **AISD** 122, 900 106 AI PIINT _906 DSP PIINT **SDRAM** DSP UNIT MC 126 156 Memory Controller 152



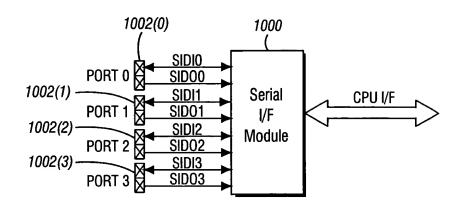


Fig. 7A EXAMPLE SERIAL INTERFACE

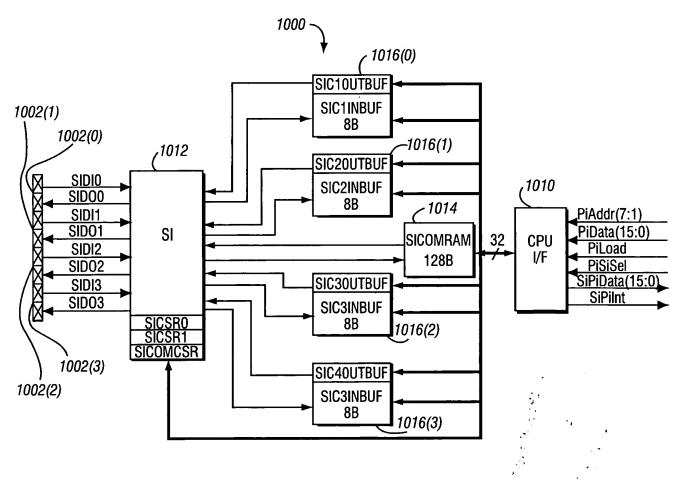


Fig. 7B EXAMPLE SERIAL INTERFACE



Register			Offset(hex)	
31	16	15	0	
SI Channel 0	Output Buffer	(SICOOUTBUF)	0x00
SI Channel 0	Input Buffer H	(SICOINBUFH)	0x04
SI Channel 0	Input Buffer L	(SICOINBUFL)		0x08
SI Channel 1	Output Buffer	(SIC10UTBUF)	0x0C
SI Channel 1	Input Buffer H	(SIC1INBUFH)	0x10
SI Channel 1	Input Buffer L	(SIC1INBUFL)		0x14
SI Channel 2	Output Buffer	(SIC2OUTBUF)	0x18
SI Channel 2	Input Buffer H	(SIC2INBUFH)	0x1C
SI Channel 2	! Input Buffer L	(SIC2INBUFL)		0x20
SI Channel 3	Output Buffer	(SIC3OUTBUF)	0x24
SI Channel 3	Input Buffer H	(SIC3INBUFH)	0x28
SI Channel 3	Input Buffer L	(SIC3INBUFL)		0x2C
SI Poll Contr	ol Register (SII	POLL)		0x30
SI Communi	cation Control	Status Registe	r (SICOMCSR)	0x34
SI Status Re	gister (SISR)			0x38
SI EXI Lock	Register (SIEXI	LK)		0x3C
SI Communi	cation RAM (1	28 Bytes)		0x80-0xFF

Fig. 7C EXAMPLE SERIAL INTERFACE REGISTERS



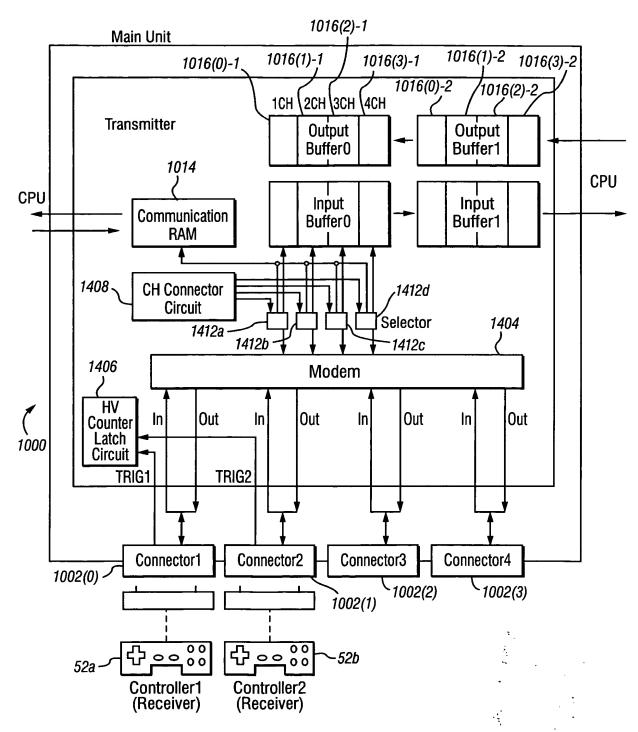


Fig. 8
EXAMPLE SERIAL INTERFACE

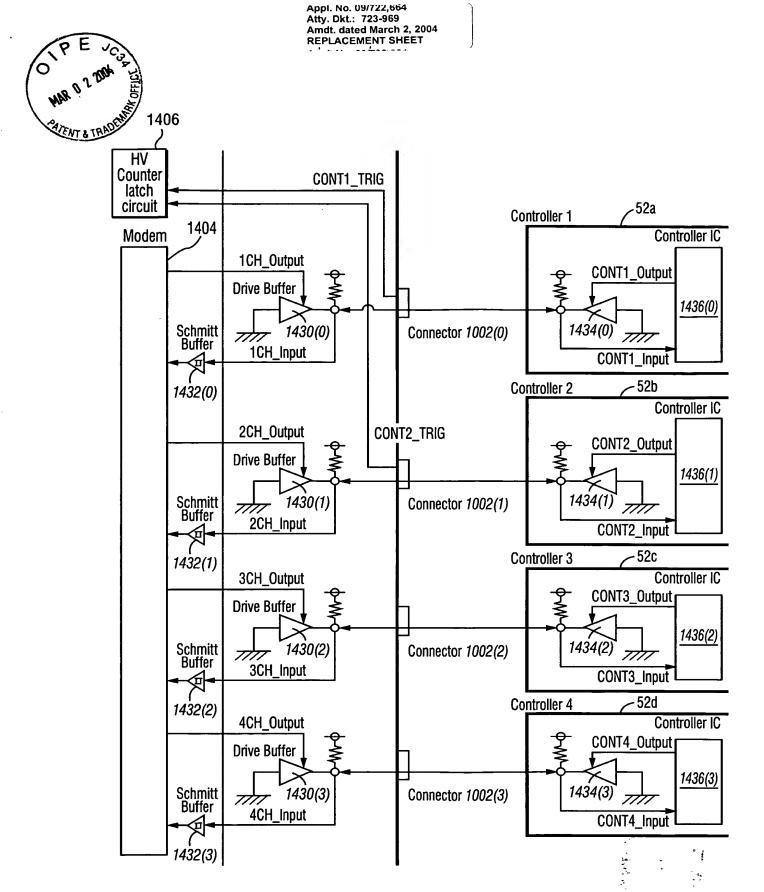
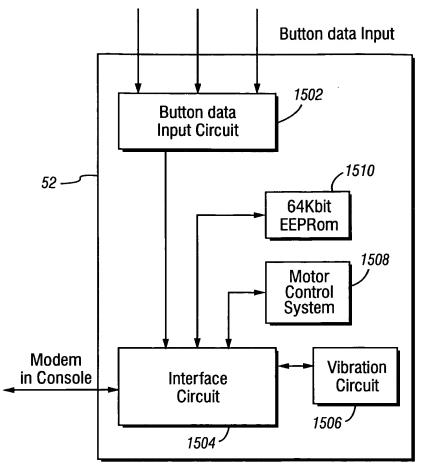


Fig. 9





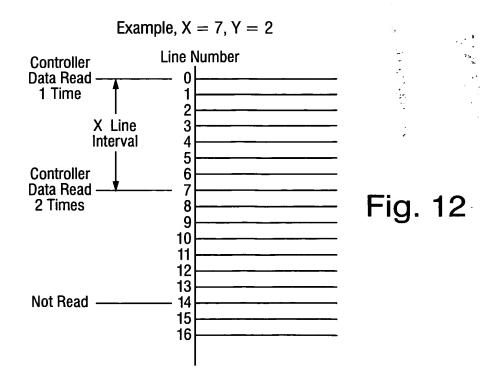


Fig. 10



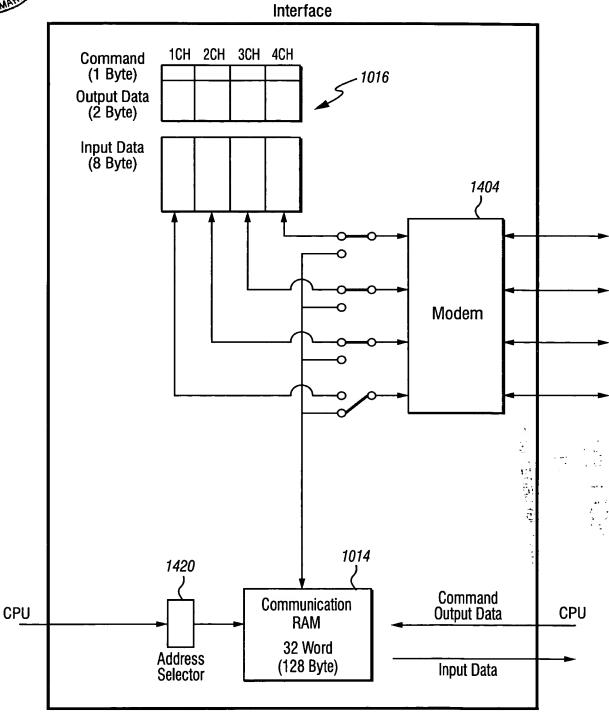
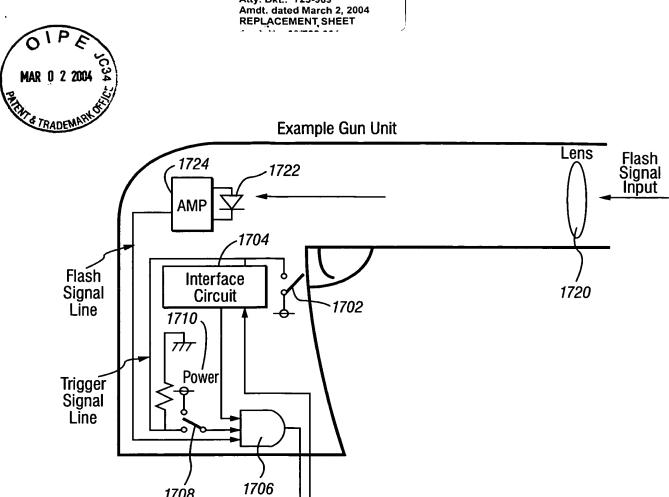


Fig. 11



1708

HV Counter Latch Circuit

Modem

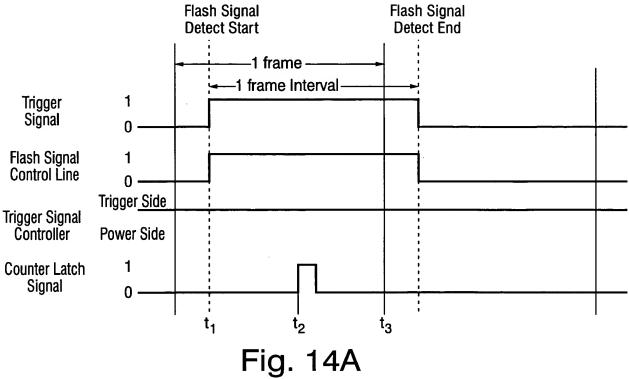
Counter Latch Signal \

f Controller has 1 line. Gun has 2 lines.

Fig. 13



Output Timing of Counter Latch Signal Gun Mode (First Type)



Output Timing of Counter Latch Signal Gun Mode (Second Type)

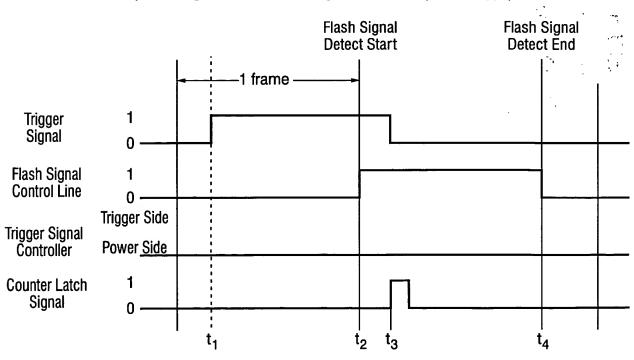


Fig. 14B



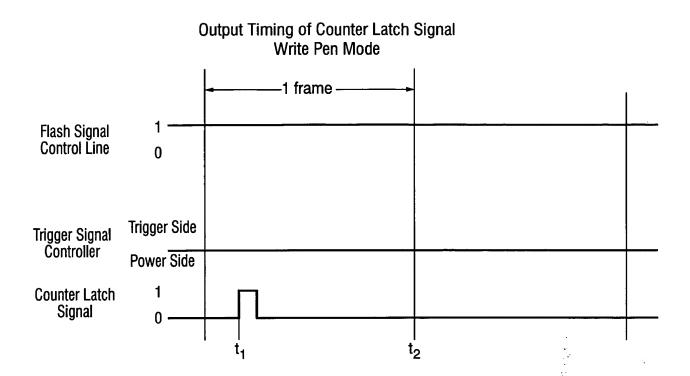


Fig. 14C



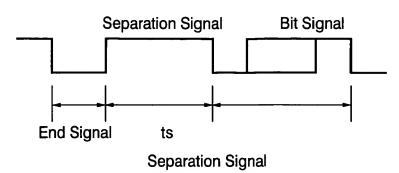
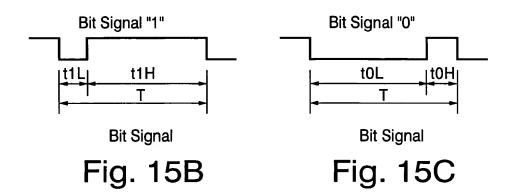


Fig. 15A



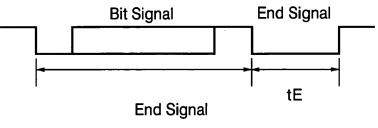


Fig. 15D

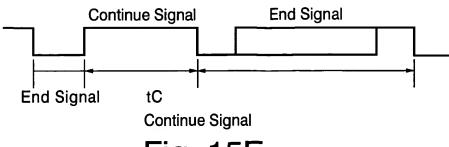


Fig. 15E



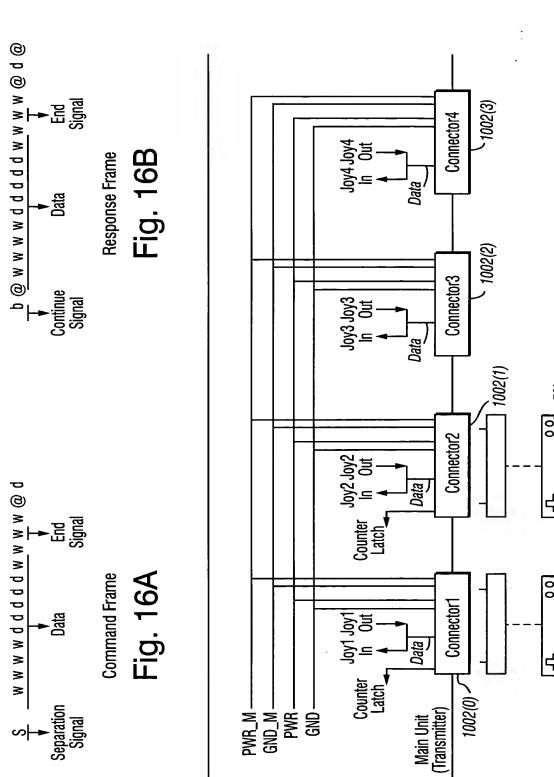
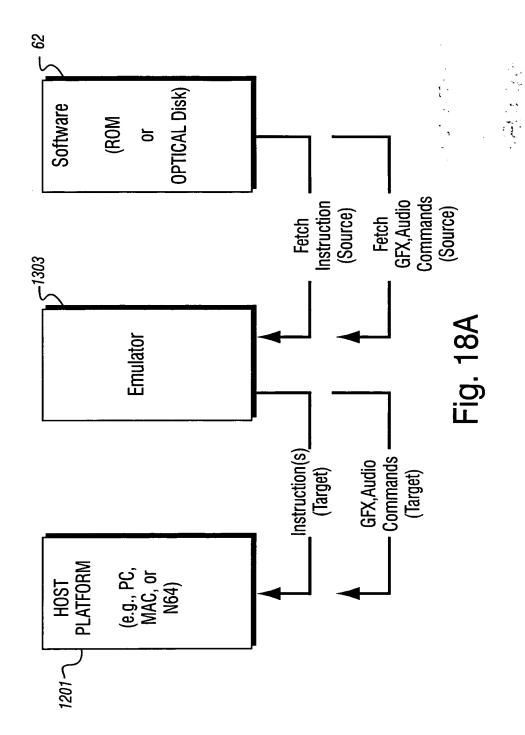


Fig. 17

Controller2 (Receiver)

Controller1 (Receiver)





Appl. No. 09/722,664 Atty. Dkt.: 723-969 Amdt. dated March 2, 2004 REPLACEMENT SHEET MAR 0 2 2004 Fig. 18B REMOTE COMPUTER MADEMARK OF MONITOR **LOCAL AREA** NETWORK 1233 1158 WIDE AREA NETWORK 1152 156 NETWORK INTERFACE 1227 1154 **KEYBOARD** 1231 SERIAL PORT INTERFACE -1235VIDEO Adapter CD-ROM Interface -1239BUS 120 SOUND **SYSTEM F** FLOPPY DISK DRIVE INTERFACE CENTRAL PROCESSING UNIT (CPU) 1209 -1221 INTERFACE 0000000 SYSTEM MEMORY 1256 APPLICATION PROGRAM 2 APPLICATION PROGRAM N OPERATING SYSTEM APPLICATION PROGRAM 1 1201 -BIOS (ROM) (RAM)

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